REMARKS

Claims 1-63 were presented for examination. Claims 1-63 were rejected. Claims 1, 15-18, 20, 22, 48, 53, 57 and 58 have been amended. Claims 46 and 47 have been canceled. Claims 64-66 have been added.

Rejections Under 35 U.S.C. § 102(b)

Claims 1-4, 15-29 and 46-57 were rejected under 35 U.S.C. § 102(b) as being anticipated by Doyle of these claims, claims 1, 15-18, 20, 22, 48, 53 and 57 are independent. Applicant respectfully traverses.

Claim 1, as amended, recites, in part, a computer system for routing of information for memory devices comprised of a central processing unit, a memory module comprised of two memory banks of substantially identical memory chips wherein a system bus connectors couples non-identical pins from each of the two memory banks. The coupled non-identical pins have internal assignments for like functions and are arranged with bilateral symmetry.

Doyle also recites an apparatus for supporting memory devices. However, Doyle fails to disclose having the pin assignments of the memory banks arranged in bilateral symmetry coupled to non-identical pin assignments between the different memory banks. Instead, Doyle discloses that all the memory banks in additional memory sockets be tied to identical pin assignments (Col. 9, lines 28-31) Further, Doyle discloses having the data and address busses (Col. 3, lines 1-2) and the memory banks (Col. 4, lines 2-5) arranged in parallel. Therefore, Applicant believes that claim 1 is not anticipated by Doyle and request the Examiner withdraw his rejection to claim 1.

Independent claims 15-18, 20 and 22 as amended, also recite coupling non-identical pins of two different memory banks with like internal function assignments in a bilateral symmetrical arrangement as called for in claim 1. Therefore, for the same reasons discussed above, Applicant believes claims 15-18, 20 and 22 are also not anticipated by Doyle, and requests that the

Examiner withdraw his rejection of claims 15-18, 20 and 22.

Claims 2-4, 19, 21 and 23-29 depend on independent claims 1, 18, 20 and 22 and are patentable for the same reasons as the independent claims from which they depend. Therefore, Applicant believes claims 2-4, 19, 21 and 23-29 are also not anticipated by Doyle, and requests that the Examiner withdraw his rejection of claims 2-4, 19, 21 and 23-29.

Claim 48, as amended, recites in part an integrated circuit memory chip comprising a circuit package that contains within it two multiplexers and a plurality of pins from a memory chip.

As mentioned above, Doyle recites an apparatus for supporting memory devices. However, Doyle fails to provide for multiplexers contained within an integrated circuit memory chip. Doyle discloses "addresses that are multiplexed externally" or mutiplexed internal to the microprocessor (Col. 3, lines 54-57). Therefore, Applicant believes that claim 48 is not anticipated by Doyle and request the Examiner withdraw his rejection to claim 48.

Independent claims 53 and 57 also recite multiplexers contained within the integrated circuit memory chip as called for in claim 48. Therefore, for the same reasons discussed above, Applicant believes claims 53 and 57 are also not anticipated by Doyle, and requests that the Examiner withdraw his rejection of claims 53 and 57.

Claims 49-52 and 54-56 depend on independent claims 48 and 53 and are patentable for the same reasons as the independent claims from which they depend. Additionally, these dependent claims recite further limitations not shown or suggested by the prior art. For example, claims 51 and 55 recite internal logic on the integrated circuit memory chip for receiving the control signal from the memory controller. In Doyle, the control signals are buffered and multiplexed between the microprocessor and the memory and, therefore, the logic is not internal to the memory itself as indicated in the claimed invention (Col. 4, lines 55-61). Applicant believes claims 49-52 and 54 -56 are also not anticipated by Doyle, and requests that the Examiner withdraw his rejection of claims 49-52, and 54 -56.

New claims 64-66 recite in part an integrated circuit memory chip comprising a memory

controller within a circuit package that contains within it two multiplexers and a plurality of pins from a memory chip.

Doyle also fails to provide for multiplexers contained within a memory controller of an integrated circuit memory chip. Doyle discloses "addresses that are multiplexed externally" or multiplexed internal to the microprocessor (Col. 3, lines 54-57). Therefore, Applicant believes that claims 64-66 is not anticipated by Doyle.

Rejections Under 35 U.S.C. § 103(a)

Claims 5, 30 and 58 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Doyle in view of well-known features of circuit packages, as further evidenced by Miller. Claim 58 is independent. Applicant respectfully traverses.

Claim 58, as amended, recites remap multiplexers that are contained within the circuit package of the memory chip. Claim 58, as amended, also recites a memory module comprised of two memory banks of substantially identical memory chips wherein a system bus connectors couples non-identical pins from each of the two memory banks. The coupled non-identical pins have internal assignments for like functions and are arranged with bilateral symmetry.

Doyle, as mentioned above, discloses an apparatus for supporting memory devices. However, Doyle fails to disclose having the pin assignments of one memory bank coupled to non-identical pin assignments to a different memory bank. Doyle also fails to disclose memory banks arranged with bilateral symmetry. Additionally, Doyle fails to disclose remap multiplexers contained within the circuit package of the memory chip itself.

Examiner admits Doyle fails to teach the use of pads and cites Miller. However, Miller fails to remedy the deficiencies of Doyle. Miller discloses memory banks comprising signal terminals that are conductive pads and that are on both sides of a circuit board. However, Miller also fails to disclose having the pin assignments of one memory banks coupled to non-identical pin assignments of a different memory bank. Miller also fails to disclose remap multiplexers

contained within the circuit package of the memory chips. Therefore, neither Doyle nor Miller disclose these limitations in the claimed invention.

Nor does the hypothetical combination of Doyle and Miller suggest or teach coupling non-identical pin assignments between the different memory banks or having remap multiplexers contained within the circuit package of the memory chips. At best, the hypothetical combination teaches memory devices with conductive pad terminals of varying sizes and shapes located on both sides of a substrate that has multiplexing performed external to the memory device. Because the hypothetical combination of Doyle and Miller does not suggest or teach all the limitations of the claimed invention. Applicant believes that claim 58 is patentable over the prior art and request the Examiner withdraw his rejection to claim 58.

Claims 5 and 30 depend from the independent claims 1 and 22 either directly or ultimately. These dependent claims are patentable for the same reasons as presented above with respect to the claims from which they depend. Therefore, Applicant asserts that claims 5 and 30 are also patentable over the prior art and requests that the Examiner withdraw his rejection thereof.

Claims 6-14, 31-45 and 59-63 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Doyle in view Miller. Applicant respectfully traverses.

Claims 6-14, 31-45 and 59-63 depend from the independent claims 1, 22 and 58 either directly or ultimately. These dependent claims are patentable for the same reasons as presented above with respect to the claims from which they depend. Therefore, Applicant asserts that claims 6-14, 31-45 and 59-63 are also patentable over the prior art and requests that the Examiner withdraw his rejection thereof.

CONCLUSION

For the above reasons, the Applicant respectfully submits that the above claims represent

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allowable subject matter. The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application or of this response. Otherwise, early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,

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